What is claimed is:

1. A method for fabricating a portion of a semiconductor device comprising:

forming a gate structure on a substrate, the gate structure including an insulating oxide layer, a nitride layer and a polysilicon layer, wherein the oxide layer is located on the substrate, the nitride layer is located on the oxide layer, and the polysilicon layer is located on the nitride layer; and

reoxidizing the gate structure to form a layer of oxide over the gate structure.

2. The method of claim 1, wherein said forming step comprises:

depositing the insulating oxide layer on the substrate;

depositing the polysilicon layer on the oxide layer;

implanting nitrogen ions into the layers; and

annealing the layers to form a nitride layer between the oxide layer and the polysilicon layer.

3. The method of claim 2, wherein the implanting step includes implanting nitrogen ions into the layers at a dose from about 1E14 ions/cm^2 to about 1E16 ions/cm^2.

4. The method of claim 2, wherein the annealing step includes annealing the layers in an inert ambient gas at a temperature from about 800°C to about 1100°C.

5. The method of claim 2, wherein the annealing step includes annealing the layers in an inert ambient gas at a temperature from about 900°C to about 1200°C using a rapid thermal process.

6. The method of claim 2, wherein the annealing step includes annealing the layers for about 15 minutes to about 60 minutes.

7. The method of claim 2, wherein the annealing step forms a nitride layer from about 10 Å to about 50 Å thick.

8. The method of claim 2, wherein the reoxidizing step includes reoxidizing the gate structure to form an oxide layer from about 25 Å to about 500 Å thick.

9. The method of claim 2, wherein prior to the reoxidizing step, forming source and drain regions in the substrate.

10. The method of claim 2, wherein the implanting step includes implanting nitrogen ions into the layers at a dose from about 1E14 ions/cm^2 to about 1E16 ions/cm^2.

11. The method of claim 10, wherein the annealing step includes annealing the layers for about 15 minutes to about 60 minutes.

12. The method of claim 11, wherein the annealing step further includes annealing the layers in an inert ambient gas at a temperature from about 800°C to about 1100°C.

13. The method of claim 11, wherein the annealing step further includes annealing the layers using rapid thermal processing in an inert ambient gas at a temperature from about 900°C to about 1200°C using a rapid thermal process.

14. The method of claim 13, wherein the inert ambient gas is argon.

15. The method of claim 13, wherein the implanting step includes implanting $^{15}N_2$+ nitrogen ions.

16. The method of claim 15, wherein the reoxidizing step includes reoxidizing the gate structure for form a oxide layer from about 25 Å to about 500 Å thick.

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17. The method of claim 1, wherein said forming step comprises:

depositing the insulating oxide layer on the substrate;

depositing the nitride layer on the oxide layer;

depositing the polysilicon layer on the nitride layer.

18. The method of claim 17, wherein the depositing step includes depositing nitride layer on the insulating oxide layer to a thickness from about 10 Å to about 50 Å.

19. The method of claim 17, wherein the reoxidizing step includes reoxidizing the gate structure to form an oxide layer from about 25 Å to about 500 Å thick.

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20. The method of claim 17, wherein the step of forming a gate structure further includes selectively etching away portions of the insulating oxide, nitride, and polysilicon layers to expose substrate and form a peripheral edge around the gate structure; and

wherein the reoxidizing step comprises exposing the substrate to an oxidizing ambient to oxidize the exposed substrate.

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21. The method of claim 20, wherein the exposing step causes an uplift in a peripheral portion of the nitride layer.

22. The method of claim 20, wherein the exposing step causes an indentation in the substrate near a peripheral edge of the gate structure.

23. The method of claim 17, wherein prior to the reoxidizing step, forming source and drain regions in the substrate.

24. A method for fabricating a portion of a semiconductor device comprising:

forming an oxide gate layer on a surface of a substrate;

forming a nitride layer on the oxide gate layer;

forming a polysilicon layer on the nitride layer;

etching away the polysilicon and nitride layers in selected areas to form a gate structure; and

reoxidizing the gate structure to form a layer of oxide.

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25. The method of claim 24, wherein the step of forming a nitride layer comprises depositing a nitride layer on the oxide gate layer.

26. The method of claim 24, wherein the step of forming a nitride layer comprises forming a nitride layer of about 10 Å to about 50 Å thick on the oxide gate layer.

27. The method of claim 24, wherein the step of reoxidizing the exposed substrate comprises reoxidizing the reoxidizing the exposed substrate to form an oxide layer from about 25 Å to about 500 Å thick.

28. The method of claim 24, wherein the step of etching exposes the surface of the substrate; and

wherein the step of reoxidizing the exposed substrate comprises exposing the substrate to an oxidizing ambient to oxidize the exposed substrate surface.

29. The method of claim 28, wherein the exposing step causes an uplift in a portion of the nitride layer proximate to a peripheral edge of the gate structure.

30. The method of claim 28, wherein the exposing step includes exposing the substrate to the oxidizing ambient at a temperature from about 650°C to about 900°C.

31. The method of claim 29, wherein the exposing step further includes exposing the substrate to the oxidizing ambient for about 10 minutes to about 60 minutes.

32. The method of claim 24, wherein prior to the reoxidizing step, forming source and drain regions in the substrate.

33. The method of claim 24, further comprising forming source and drain regions in the substrate after the reoxidizing step.

34. A method for fabricating a portion of a semiconductor device comprising:

forming an oxide layer on a substrate;

forming a polysilicon layer on the oxide layer;

implanting a nitrogen ion into the oxide and polysilicon layers;

annealing the oxide and polysilicon layers to form a nitride layer between the oxide and polysilicon layers;

etching the polysilicon, nitride, and oxide layers to expose the substrate and form a gate structure; and

reoxidizing the exposed substrate and the gate structure.

35. The method of claim 34, wherein the implanting step includes implanting nitrogen ions into the layers at a dose from about 1E14 ions/cm^2 to about 1E16 ions/cm^2.

36. The method of claim 34, wherein the implanting step includes implanting $^{15}N_2+$ nitrogen ions into the layers.

37. The method of claim 34, wherein the annealing step further includes annealing the layers in an inert ambient gas at a temperature from about 800°C to about 1100°C.

38. The method of claim 34, wherein the annealing step further includes annealing the layers using rapid thermal processing in an inert ambient gas at a temperature from about 900°C to about 1200°C.

39. The method of claim 34, wherein the annealing step includes annealing the layers for about 15 minutes to about 60 minutes.

40. The method of claim 34, wherein the annealing step forms a nitride layer from about 10 Å to about 50 Å thick

41. The method of claim 34, wherein the etching step further includes creating a peripheral edge around the gate structure.

42. The method of claim 41, wherein the step of reoxidizing the exposed substrate comprises exposing the substrate to an oxidizing ambient to oxidize the exposed substrate.

43. The method of claim 42, wherein the exposing step causes an uplift in a portion of the nitride layer proximate to the peripheral edge.

44. The method of claim 34, wherein prior to the reoxidizing step, forming source and drain regions in the substrate.

45. The method of claim 34, further comprising forming source and drain regions in the substrate after the reoxidizing step.

46. An integrated circuit device comprising:

a substrate;

a gate structure, wherein the gate structure includes:

a gate oxide layer on the substrate,

a nitride layer on the gate oxide layer, and

a polysilicon layer over the nitride layer;

a channel region under the gate structure; and

source/drain regions in the substrate adjacent the channel region.

47. The integrated circuit device of claim 46, wherein the nitride layer is from about 10 Å to about 50 Å thick.

48. The integrated circuit device of claim 46, wherein the nitride layer is deposited over said gate oxide layer.

49. The integrated circuit device of claim 46, wherein the nitride layer is formed by nitrogen implantation to form an implanted area and by annealing of the implanted area.

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50. The integrated circuit device of claim 46, wherein the gate has ~~a peripheral edge and further including an~~ uplift in the nitride layer occurring in portions of the nitride layer proximate the peripheral edge of the gate structure, the uplift caused by reoxidation of the gate structure, wherein asperities are absent from the polysilicon layer.

51. The integrated circuit device of claim 46, wherein the substrate has a surface and further including an indentation in the surface of the substrate located proximate to the peripheral edge of the gate, the indentation resulting from reoxidation of the integrated circuit device.

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52. The integrated circuit device of claim 46 further wherein the gate structure includes sidewall spacers located on each edge of the gate structure and lightly doped drain regions in the substrate located in the substrate below the sidewall spacers.

53. The integrated circuit device of claim 46, wherein the substrate is a p-type substrate and wherein the source/drain regions are formed by implanting n-type impurities in the p-type substrate.

54. The integrated circuit device of claim 53, wherein the source/drain regions are implanted prior to reoxidation.

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55. The integrated circuit device of claim 53, wherein the source/drain regions are implanted after oxidation.

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